CLAIMS

What is claimed is:

1. A multiplexer circuit, comprising:

a first plurality of circuit input terminals providing a first plurality of input signals;

a second plurality of circuit input terminals providing a second plurality of input signals having complementary values to the first plurality of input signals;

a circuit output terminal;

a first multiplexer having a plurality of input terminals coupled to the first plurality of circuit input terminals, at least one select terminal, and an output terminal;

a second multiplexer having a plurality of input terminals coupled to the second plurality of circuit input terminals, at least one select terminal coupled to the at least one select terminal of the first multiplexer, and an output terminal; and

an output circuit having a first input terminal coupled to the output terminal of the first multiplexer, a second input terminal coupled to the output terminal of the second multiplexer, and an output terminal coupled to the circuit output terminal,

wherein the first and second multiplexers are configured to select a corresponding one of their respective input terminals in response to equivalent signals received at their respective select terminals.

2. The multiplexer circuit of Claim 1, further comprising a plurality of inversion circuits, each inversion circuit being coupled between one of the first circuit input terminals and a corresponding one of the second circuit input terminals.

3. The multiplexer circuit of Claim 2, wherein each of the inversion circuits comprises an inverter.

4. The multiplexer circuit of Claim 2, wherein each of the inversion circuits comprises a memory cell.

5. The multiplexer circuit of Claim 2, wherein each of the inversion circuits comprises a pulldown coupled between a corresponding one of the second circuit input terminals and a ground terminal, each of the inversion circuits having a gate terminal coupled to a corresponding one of the first circuit input terminals.

6. The multiplexer circuit of Claim 1, further comprising a plurality of memory cells, each memory cell having a true output terminal coupled to one of the first plurality of circuit input terminals and a complement output terminal coupled to a corresponding one of the second plurality of circuit input terminals.

7. The multiplexer circuit of Claim 1, further comprising at least one memory cell coupled to the select terminals of the first and second multiplexers.

8. The multiplexer circuit of Claim 1, wherein:

each of the first and second multiplexers comprises a plurality of select terminals comprising select terminal pairs; and

the multiplexer circuit further comprises, for each select terminal pair, an inverter coupled between the two select terminals comprising the pair.

9. The multiplexer circuit of Claim 1, wherein the output circuit comprises a latch.

10. The multiplexer circuit of Claim 9, wherein the latch comprises first and second cross-coupled inverters.

11. The multiplexer circuit of Claim 1, wherein the output circuit comprises:

an inverter having an input terminal coupled to the output terminal of the first multiplexer and an output terminal coupled to the circuit output terminal;

a first pullup coupled between the output terminal of the first multiplexer and a power high terminal, the first pullup having a gate terminal coupled to the output terminal of the second multiplexer; and

a second pullup coupled between the output terminal of the second multiplexer and the power high terminal, the second pullup having a gate terminal coupled to the output terminal of the first multiplexer.

12. The multiplexer circuit of Claim 1, wherein the output circuit comprises:

an inverter having an input terminal coupled to the output terminal of the second multiplexer and an output terminal coupled to the output terminal of the first multiplexer; and

a P-channel transistor coupled between the output terminal of the second multiplexer and a power high terminal, the P-channel transistor having a gate terminal coupled to the output terminal of the first multiplexer and further coupled to the circuit output terminal.

13. The multiplexer circuit of Claim 1, wherein the first and second pluralities of circuit input terminals each comprise eight input terminals.

14. The multiplexer circuit of Claim 1, wherein the first and second multiplexers each comprise a plurality of transistors coupled in series between their respective input and output terminals, and all of the transistors consist of N-channel transistors.

15. The multiplexer circuit of Claim 1, wherein the first and second multiplexers comprise binary multiplexers.

16. The multiplexer circuit of Claim 1, wherein the first and second multiplexers comprise one-hot multiplexers.

17. A multiplexer circuit, comprising:

a plurality of circuit input terminals;

a circuit output terminal;

a first multiplexer having a plurality of input terminals coupled to the circuit input terminals, at least one select terminal, and an output terminal;

a second multiplexer having a plurality of input terminals, at least one select terminal coupled to the at least one select terminal of the first multiplexer, and an output terminal;

a plurality of pulldowns, each pulldown being coupled between a ground terminal and a corresponding one of the input terminals of the second multiplexer, each pulldown having a gate terminal coupled to a corresponding one of the circuit input terminals; and

an output circuit having a first input terminal coupled to the output terminal of the first multiplexer, a second input terminal coupled to the output terminal of the second multiplexer, and an output terminal coupled to the circuit output terminal,

wherein the first and second multiplexers are configured to select a corresponding one of their respective input terminals in response to equivalent signals received at their respective select terminals.

18. The multiplexer circuit of Claim 17, further comprising at least one memory cell coupled to the select terminals of the first and second multiplexers.

19. The multiplexer circuit of Claim 17, wherein:

each of the first and second multiplexers comprises a plurality of select terminals comprising select terminal pairs; and

the multiplexer circuit further comprises, for each select terminal pair, an inverter coupled between the two select terminals comprising the pair.

20. The multiplexer circuit of Claim 17, wherein the output circuit comprises a latch.

21. The multiplexer circuit of Claim 20, wherein the latch comprises first and second cross-coupled inverters.

22. The multiplexer circuit of Claim 17, wherein the output circuit comprises:

an inverter having an input terminal coupled to the output terminal of the first multiplexer and an output terminal coupled to the circuit output terminal;

a first P-channel transistor coupled between the output terminal of the first multiplexer and a power high terminal, the P-channel transistor having a gate terminal coupled to the output terminal of the second multiplexer; and

a second P-channel transistor coupled between the output terminal of the second multiplexer and the power high terminal, the P-channel transistor having a gate terminal coupled to the output terminal of the first multiplexer.

23. The multiplexer circuit of Claim 17, wherein the output circuit comprises:

an inverter having an input terminal coupled to the output terminal of the second multiplexer and an output terminal coupled to the output terminal of the first multiplexer; and

a P-channel transistor coupled between the output terminal of the second multiplexer and a power high terminal, the P-channel transistor having a gate terminal coupled to the output terminal of the first multiplexer and further coupled to the circuit output terminal.

24. The multiplexer circuit of Claim 17, wherein the plurality of circuit input terminals comprises eight input terminals.

25. The multiplexer circuit of Claim 17, wherein the first and second multiplexers each comprise a plurality of transistors coupled in series between their respective input and output terminals, and all of the transistors consist of N-channel transistors.

26. The multiplexer circuit of Claim 17, wherein the first and second multiplexers comprise binary multiplexers.

27. The multiplexer circuit of Claim 17, wherein the first and second multiplexers comprise one-hot multiplexers.

28. A lookup table (LUT) for a programmable logic device (PLD), comprising:

a plurality of configuration memory cells for the PLD, each configuration memory cell having a true output terminal and a complement output terminal;

a plurality of LUT input terminals;

a LUT output terminal;

a first multiplexer having a plurality of input terminals coupled to the true output terminals of the configuration memory cells, a plurality of select terminals coupled to the plurality of LUT input terminals, and an output terminal;

a second multiplexer having a plurality of input terminals coupled to the complement output terminals of the configuration memory cells, a plurality of select terminals coupled to the plurality of LUT input terminals, and an output terminal; and

an output circuit having a first input terminal coupled to the output terminal of the first multiplexer, a second input terminal coupled to the output terminal of the second multiplexer, and an output terminal coupled to the LUT output terminal,

wherein the first and second multiplexers are configured to select a corresponding one of their respective input terminals in response to equivalent signals received at their respective select terminals.

29. The LUT of Claim 28, wherein:

for each of the first and second multiplexers, the select terminals comprise select terminal pairs; and

the LUT further comprises, for each select terminal pair, an inverter coupled between the two select terminals comprising the pair.

30. The LUT of Claim 28, wherein the output circuit comprises a latch.

31. The LUT of Claim 30, wherein the latch comprises first and second cross-coupled inverters.

32. The LUT of Claim 28, wherein the output circuit comprises:

an inverter having an input terminal coupled to the output terminal of the first multiplexer and an output terminal coupled to the circuit output terminal;

a first pullup coupled between the output terminal of the first multiplexer and a power high terminal, the first pullup having a gate terminal coupled to the output terminal of the second multiplexer; and

a second pullup coupled between the output terminal of the second multiplexer and the power high terminal, the second pullup having a gate terminal coupled to the output terminal of the first multiplexer.

33. The LUT of Claim 28, wherein the output circuit comprises:

an inverter having an input terminal coupled to the output terminal of the second multiplexer and an output terminal coupled to the output terminal of the first multiplexer; and

a P-channel transistor coupled between the output terminal of the second multiplexer and a power high terminal, the P-channel transistor having a gate terminal coupled to the output terminal of the first multiplexer and further coupled to the circuit output terminal.

34. The LUT of Claim 28, wherein the first and second pluralities of circuit input terminals each comprise eight input terminals.

35. The LUT of Claim 28, wherein the first and second multiplexers each comprise a plurality of transistors coupled in series between their respective input and output terminals, and all of the transistors consist of N-channel transistors.

36. The LUT of Claim 28, wherein the first and second multiplexers comprise binary multiplexers.

37. The LUT of Claim 28, wherein the first and second multiplexers comprise one-hot multiplexers.

38. A programmable logic device (PLD), comprising:

a programmable interconnect structure; and

a plurality of lookup tables (LUTs) programmably interconnected by the programmable interconnect structure,

wherein each of the LUTs comprises:

a plurality of configuration memory cells for the PLD, each configuration memory cell having a true output terminal and a complement output terminal;

a plurality of LUT input terminals programmably coupled to the programmable interconnect structure;

a LUT output terminal programmably coupled to the programmable interconnect structure;

a first multiplexer having a plurality of input terminals coupled to the true output terminals of the configuration memory cells, a plurality of select terminals coupled to the plurality of LUT input terminals, and an output terminal;

a second multiplexer having a plurality of input terminals coupled to the complement output terminals of the configuration memory cells, a plurality of select terminals coupled to the plurality of LUT input terminals, and an output terminal; and

an output circuit having a first input terminal coupled to the output terminal of the first multiplexer, a second input terminal coupled to the output terminal of the second multiplexer, and an output terminal coupled to the LUT output terminal,

wherein the first and second multiplexers are configured to select a corresponding one of their respective input terminals in response to equivalent signals received at their respective select terminals.

39. A routing multiplexer for programmably coupling interconnect lines in a programmable logic device (PLD), the routing multiplexer comprising:

a plurality of configuration memory cells for the PLD;

a plurality of circuit input terminals coupled to a plurality of the interconnect lines;

a circuit output terminal coupled to one of the interconnect lines;

a first multiplexer having a plurality of input terminals coupled to the circuit input terminals, a plurality of select terminals coupled to the configuration memory cells, and an output terminal;

a second multiplexer having a plurality of input terminals, a plurality of select terminals coupled to the select terminals of the first multiplexer, and an output terminal;

a plurality of inversion circuits, each inversion circuit being coupled between one of the circuit input terminals and a corresponding one of the input terminals of the second multiplexer; and

an output circuit having a first input terminal coupled to the output terminal of the first multiplexer, a second input terminal coupled to the output terminal of the second multiplexer, and an output terminal coupled to the circuit output terminal,

wherein the first and second multiplexers are configured to select a corresponding one of their respective input terminals in response to equivalent signals received at their respective select terminals.

40. The routing multiplexer of Claim 39, wherein each of the inversion circuits comprises an inverter.

41. The routing multiplexer of Claim 39, wherein each of the inversion circuits comprises a pulldown coupled between a ground terminal and a corresponding one of the input terminals of the second multiplexer, each pulldown having a gate terminal coupled to a corresponding one of the circuit input terminals.

42. The routing multiplexer of Claim 39, wherein:

for each of the first and second multiplexers, the select terminals comprise select terminal pairs; and

the routing multiplexer further comprises, for each select terminal pair, an inverter coupled between the two select terminals comprising the pair.

43. The routing multiplexer of Claim 39, wherein the output circuit comprises a latch.

44. The routing multiplexer of Claim 43, wherein the latch comprises first and second cross-coupled inverters.

45. The routing multiplexer of Claim 39, wherein the output circuit comprises:

an inverter having an input terminal coupled to the output terminal of the first multiplexer and an output terminal coupled to the circuit output terminal;

a first pullup coupled between the output terminal of the first multiplexer and a power high terminal, the first pullup having a gate terminal coupled to the output terminal of the second multiplexer; and

a second pullup coupled between the output terminal of the second multiplexer and the power high terminal, the second pullup having a gate terminal coupled to the output terminal of the first multiplexer.

46. The routing multiplexer of Claim 39, wherein the output circuit comprises:

an inverter having an input terminal coupled to the output terminal of the second multiplexer and an output terminal coupled to the output terminal of the first multiplexer; and

a P-channel transistor coupled between the output terminal of the second multiplexer and a power high terminal, the P-channel transistor having a gate terminal coupled to the output terminal of the first multiplexer and further coupled to the circuit output terminal.

47. The routing multiplexer of Claim 39, wherein the first and second pluralities of circuit input terminals each comprise eight input terminals.

48. The routing multiplexer of Claim 39, wherein the first and second multiplexers each comprise a plurality of transistors coupled in series between their respective input and output terminals, and all of the transistors consist of N-channel transistors.

49. The routing multiplexer of Claim 39, wherein the first and second multiplexers comprise binary multiplexers.

50. The routing multiplexer of Claim 39, wherein the first and second multiplexers comprise one-hot multiplexers.

51. A programmable logic device (PLD), comprising:

a plurality of configurable logic blocks;

a plurality of interconnect lines programmably coupled to the configurable logic blocks; and

a plurality of programmable routing multiplexers interconnecting the plurality of interconnect lines,

wherein each programmable routing multiplexer comprises:

a plurality of configuration memory cells for the PLD;

a plurality of circuit input terminals coupled to a plurality of the interconnect lines;

a circuit output terminal coupled to one of the interconnect lines;

a first multiplexer having a plurality of input terminals coupled to the circuit input terminals, a plurality of select terminals coupled to the configuration memory cells, and an output terminal;

a second multiplexer having a plurality of input terminals, a plurality of select terminals coupled to the select terminals of the first multiplexer, and an output terminal;

a plurality of inversion circuits, each inversion circuit being coupled between one of the circuit input terminals and a corresponding one of the input terminals of the second multiplexer; and

an output circuit having a first input terminal coupled to the output terminal of the first multiplexer, a second input terminal coupled to the output terminal of the second multiplexer, and an output terminal coupled to the circuit output terminal,

wherein the first and second multiplexers are configured to select a corresponding one of their respective input terminals in response to equivalent signals received at their respective select terminals.

52. A method of selecting one from a plurality of circuit input signals, comprising:

providing the circuit input signals to a first multiplexer;

generating a plurality of complementary input signals from the circuit input signals, the complementary input signals having a first value whenever corresponding ones of the circuit input signals have a second value;

providing the complementary input signals to a second multiplexer;

selecting one of the circuit input signals in the first multiplexer and a corresponding one of the complementary input signals in the second multiplexer; and

utilizing the selected signals to generate an output signal.

53. The method of Claim 52, wherein the first value is a low value and the second value is a high value.

54. The method of Claim 52, wherein the complementary input signals are strict inversions of the corresponding circuit input signals.

55. The method of Claim 52, wherein selecting one of the circuit input signals in the first multiplexer and a corresponding one of the complementary input signals in the second multiplexer comprises utilizing values stored in memory cells to control the selecting.

56. The method of Claim 55, wherein the method is performed in a programmable logic device (PLD), and the memory cells are configuration memory cells of the PLD.

57. The method of Claim 56, wherein the method is performed by a programmable routing multiplexer of the PLD.

58. The method of Claim 52, further comprising storing the circuit input signals in a plurality of memory cells.

59. The method of Claim 58, wherein the method is performed in a programmable logic device (PLD), and the memory cells are configuration memory cells of the PLD.

60. The method of Claim 59, wherein the method is performed by a programmable lookup table (LUT) of the PLD.